Remarks

The Office Action dated July 9, 2010 presents the following rejections: claims 1, 3-4, 8 and 10 stand rejected under 35 U.S.C. § 103(a) over Dally (U.S. Patent No. 6,192,384) in view of Garde (U.S. Patent No. 6,510,510); and claims 2, 5-7, 9, 11 and 12 stand rejected under 35 U.S.C. § 103(a) over the '384 and '510 references in further view of Fisher (U.S. Patent No. 6,026,479). Applicant traverses all of the rejections and, unless stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

Applicant respectfully traverses the § 103(a) rejections because the cited '384 reference either alone or in combination with the '510 and '479 references lacks correspondence and teaches away from the proposed embodiment. As acknowledged in the Office Action the '384 reference fails to disclose aspects regarding, *e.g.,* a multi-issue process including a second set of issue slots that have holdable registers on the single data input path of an input routing network and that do not have holdable registers on the multiple data output paths of the input routing network. The '510 and '479 references fail to cure these deficiencies. As explained below, technical flaws of the proposed embodiment prevent the system from correctly receiving and processing operands. Accordingly, the references teach away from the proposed combination and correspondence is not shown.

Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('384) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). The primary purpose of each of the references is to execute processor operations (see Abstracts). As described below, technical flaws of the proposed embodiment prevent ALUs from receiving and processing operands, thus, undermining the operation and the purpose of the references.

The Office Action supposes that the skilled artisan would somehow utilize the cross-point switch 30 of the '384 reference to route data values from latch 130 of the '510

reference to the computation circuits 150 of the '510 reference without using the registers (as shown in the '384 reference) to buffer the data values output from the cross-point switch before inputting them to the computation circuits. In this manner, the Examiner asserts that "the holdable registers [(asserted latch 130)] of the combined issue slot(s) are on the single input path of the input routing network and not on the final output paths of the input routing network." However, the Examiner's proposed combination ignores the functional limitations of the cross-point switch and requirements of computation circuits. Specifically, the cross-point switch can only route one data value at a time, and the computation circuit 150 requires two values to be presented to respective inputs of the circuit simultaneously.

As shown by Figure 2 of the '384 reference (reproduced below), registers 28 are used at the cross-point switch 30 outputs to buffer a first data value to a first input of an ALU 26 while routing a second data value to a second ALU input. It should be apparent to one skilled in the art that, without buffering, the first data value would change when the cross-point switch 30 is re-configured to route the second data value. A large majority of ALU operations, including those intended by the '384 reference, require two operands for input (*See, e.g.* Figure 3, disclosing +,*, and / operations). Because these basic operations cannot be performed, Applicant submits that the embodiment does not function as a processing system (*i.e.*, the primary purpose of each reference). *See, e.g.,* M.P.E.P. § 2143.01 ("If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious."). Accordingly, the references teach away from such a modification and the rejections cannot be maintained.

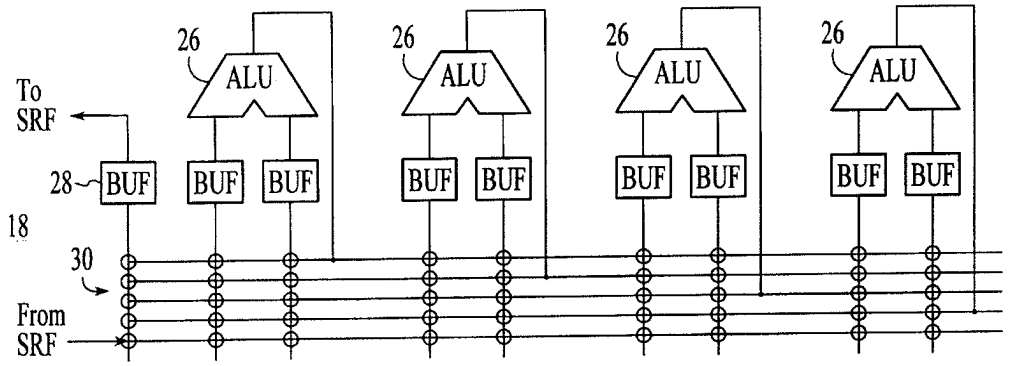

FIG. 2

More specifically, aspects of the claimed invention are directed to particular placements of holdable registers within a multi-issue processor. As discussed in Applicant's disclosure, multi-issue processors contain multiple functional units. Depending upon the current instruction, one or more of the functional units might not be used each cycle. Thus, one aspect of the invention uses a first set of issue slots that have holdable registers located at the input of the functional units (*see, e.g.,* Figure 2). Thus, when a functional unit is not used, the input remains constant, thereby reducing power consumption of the functional unit. Other aspects of the present invention recognize that when an interrupt event occurs, the presence of such holdable registers means that a large amount of data needs to be stored before the interrupt event can be processed. Thus, a second set of issue slots have holdable registers implemented before a routing network (*see, e.g.,* Figure 3) and do not have holdable registers located at the input of each of the functional units. The routing network provides multiple data outputs for a single data input and therefore, the total number of registers is less when placed before the routing network. The second set of holdable registers can, for example, be used in connection with an issue slot that is associated with interrupts (*see, e.g.,* claim 5).

Turning now to the cited references, neither the '384 reference nor the '510 reference teach issue slots that have holdable registers on the single data input path of an input routing network and that do not have holdable registers on the multiple data output paths of the input routing network, as in the claimed invention. For example, the '384 reference teaches that each of ALU clusters 18 (*i.e.,* the asserted issue slots) uses the same configuration of buffers 28 (*i.e.,* the asserted holdable registers) with a buffer 28 being located on each output of cross point switch 30 (*i.e.,* the asserted outputs of the input routing network) in each of the ALU clusters 18. *See, e.g.,* Figures 1 and 2. Thus, the '384 reference does not teach issue slots that do not have holdable registers on the multiple data output paths of the input routing network as claimed. Applicant submits that the '510 reference also fails to teach such aspects of the claimed invention. Instead, the '510 reference teaches that each of computational blocks 12 and 14 (*i.e.,* the asserted issue slots) uses the same configuration of latches (*i.e.,* the asserted holdable registers) with a latch 132 being located on the input to buses 110 and 112 and latches 160 and 165 located on the outputs of the buses 110 and 112 (*i.e.,* the asserted outputs of the input routing network) in

each of the computational blocks 12 and 14. *See, e.g.,* Figures 1 and 2. As such, the '384 reference also does not teach issue slots that do not have holdable registers on the multiple data output paths of the input routing network as claimed.

Applicant further traverses the § 103 rejections because the Examiner has not presented any motivation to modify the embodiments disclosed by the references to have two sets of issue slot architectures with different holdable register placement. The record suggests that the Examiner has impermissibly used Applicant's teachings as the basis for the conclusion of obviousness. In each of the cited references, the identical issue slots are used. The Examiner has not presented any support or explanation why one skilled in the art would be motivated to modify some but not all of the issue slots of an embodiment. Absent Applicant's specification, there is nothing in the record that would suggest to the skilled artisan to include these aspects. Applicant submits that the Examiner has simply identified registers, functioning units, and registers as elements, which can be found in any number of references, and then arranged these aspects using the claimed invention as a template. This is the hallmark of improper hindsight reconstruction with the proposed combination being derived, not "on the basis of the facts gleaned from the prior art," but solely from Applicant's disclosure. *See, e.g.,* M.P.E.P. § 2142. Accordingly, the rejections are improper and Applicant requests that they be reversed.

In view of the above, the § 103(a) rejections are improper and Applicant requests that they be withdrawn. New claims 13 through 17 are believed to be allowable for reasons similar to the above. Support for these new claims can be found at least at paragraphs 0018-0020 of Applicant's published application as well as throughout Applicant's specification.

In view of the above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, David Schaeffer, of NXP Corporation at (408) 474-9068 (or the undersigned).

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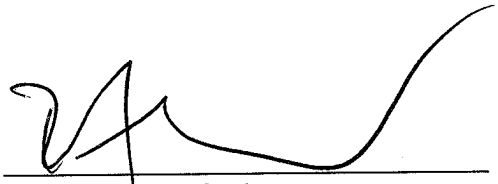
By: 

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